

REMARKS

Claims 1-9 and 11-28 are pending in the application at hand, which is a continuation of U.S. Application No. 09/713,732 (now U.S. Patent No. 6,173,247).

The Specification has been objected to because the information in the Related Applications section does not reflect the current patent numbers associated with application numbers 09/713,732 and 09/096,774. The Specification is being amended in the Amendments to the Specification section above to include the current patent numbers.

Claims 8 and 18 have been objected to under 37 C.F.R. 1.75(d)(1) because the phrase “indicating number of times” is understood to mean “indicating *the* number of times.” Claims 8 and 18 are being amended to insert the article “the” before the term “number.”

Claims 1-9 and 11-28 have been rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

According to M.P.E.P. 2106(IV)(B)(2)(B)(ii), for a computer process to be statutory,

the claimed process must be limited to a practical application of [an] abstract idea or mathematical algorithm in the technological arts. . . . A claim is limited to a practical application when the method, as claimed, produces a concrete, tangible and useful result; i.e., the method recites a step or act of producing something that is concrete, tangible and useful.

For example, the Federal Circuit held in the State Street Bank case that,

the transformation of data, representing discrete dollar amounts by a machine through a series of mathematical calculations into a final share price, constitutes a practical application of the mathematical algorithm, formula, or calculation because it produces ‘a useful, concrete, and tangible result’-- a final share price momentarily fixed for recording and recording purposes and even accepted and relied upon by regulatory authorities and in subsequent trades.

See Interim Guidelines for Examination of Patent Applications for Patent Subject Matter Eligibility, page 39, at

http://www.uspto.gov/web/offices/pac/dapp/opla/preognotice/guidelines101_20051026.pdf.

Applicants provide a method of modeling a digital processor to reduce the development time of going from a floating-point model to the real-time implementation of a given operation or function on a fixed-point digital processor. See Specification as originally filed, page 2, lines 2-10. Referring to Fig. 10 of the drawings, operations 29, such as addition, multiplication, subtraction, and so forth, and data representations 27 of the operands for the operations 29 of the digital processor are defined in a high level programming language and are loaded in a computer system. The defined operations 29 and data representations 27 are used in commands for execution by a target processor 19.

The computer system uses the operations 29 and data representations 27 to simulate the target processor 19 executing certain commands (e.g., code or operations 25) to provide a model (e.g., fixed-point model 15) of the target processor 19. The simulation includes generating model data ("output model") 21 indicative of results of the target processor 19 having executed the certain commands (e.g., code or operations 25). The generated model data 21 provides a bit level representation of the target processor results ("output target") 23.

The method also includes executing working code on the target processor 19 to generate working data (i.e., output target 23). In simulation, the model 15 generates model data 21 that corresponds to the working data in a manner such that the model data 21 is bit-wise matchable to the working data 23.

Applicants' method of now amended claim 1 produces a model that is a concrete, tangible, and useful result because it is used to decrease development time for the real-time implementation of given operations or functions on a fixed-point DSP and thereby narrows an advantageous gap between software development for floating-point DSPs and fixed-point DSPs (see Specification, page 2, lines 9-12). Indeed, Applicants' claimed method is similar to the computer process in the State Street Bank case in which the Federal Circuit determined that the computer process is statutory subject matter under 35 U.S.C. 101. As described above, the computer process in State Street Bank performed a series of mathematical calculations to obtain a final share price useful for recording purposes and relied upon by regulatory authorities. Similarly, Applicants' claimed method performs simulations to obtain a model useful for reducing development time for the real-time implementation of operations or functions on a target processor.

Therefore, now amended claim 1 achieves a practical application with a useful, concrete and tangible result (“to decrease development time of a real-time implementation of the certain commands on the target processor”). Accordingly, Applicants respectfully submit that the rejection of claim 1 under 35 U.S.C. 101 is improper and should be withdrawn. Because independent claims 11 and 20 are being amended in a similar manner, they should be allowed for similar reasons. Since claims 2-9 depend from base claim 1, claims 12-19 depend from base claim 11, and 21-28 depend from base claim 20, these claims should be allowed for at least the same reasons.

Claims 1-9 and 11-28 have been rejected under the judicially created doctrine of obviousness-type double patenting in view of U.S. Patent No. 6,741,958. To overcome this rejection, as stated on page 5 of the Office Action, a Terminal Disclaimer in compliance with 37 C.F.R. 1.321 is co-filed herewith. Acceptance is respectfully requested.

CONCLUSION

In view of the above amendments and remarks, it is believed that all now pending claims (claims 1-9 and 11-28) are in condition for allowance, and it is respectfully requested that the application be passed to issue. If the Examiner feels that a telephone conference would expedite prosecution of this case, the Examiner is invited to call the undersigned.

Respectfully submitted,

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